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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/824,751	04/04/2001	Hiroki Koike	Q63945	9722

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EXAMINER	
ABRAHAM, ESAW T	

ART UNIT	PAPER NUMBER
2133	9

DATE MAILED: 11/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/824,751	Applicant(s) KOIKE, HIROKI	
	Examiner Esaw T Abraham	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4, 6-8* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims **1 to 10** are presented for examination.

****** The examiner considers the preliminary amendment filled on 04/04/01.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No: 2000-103568 filed on 04/05/2000.

Information Disclosure Statement

3. The references listed in the information disclosure statement submitted on 04/04//01, 04/09/03, 06/13/03 and 08/06/03 have been considered by the examiner (see attached PTO-1449).

Claim objections

4. a) Claims 4 and 9 are objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim should refer to other claims in the alternative only---, and/or, ---cannot depend from any other multiple dependent claim. See MPEP § 608.01(n). Accordingly, the claim has not been further treated on the merits.

Appropriate correction is required.

b) Claim 10 is objected to under 37 CFR 1.75(c) as being in improper form:

Please change the phrase "characterized in the system comprises the steps of" to " characterized in the system comprises" in lines 7 and 8 of claim 10.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Rejection under 35 U.S.C. 102(e), Patent to Another with earlier Filing date, Reference is a U.S. Patent Issued Directly or Indirectly From a National Stage of, or a Continuing Application Claiming benefit under 35 U.S.C. 365© to, an International Application Having an International Filling Date Prior to November 29, 2000.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims **1, 2, 4-7, 9, and 10,** are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Yamada et al. (U.S. PN: 6,091,65).

As per claim **1,** Yamada et al. teach or disclose a semiconductor memory comprising an information memory cells (see fig. 1(a) and col. 4, lines 40-65) for storing and performing operations of reading out information, a word line for accessing the memory cell, and a reference memory cell other than the information memory cell coupled to the word line or to a word line having the same address as the word line wherein the reference memory cell stores information for use by a sense amplifier, the information being reference information equivalent to a

reference potential to the reading of information from the information memory cell (see col. 2, lines 17-40). Yamada et al. further, teach that the semiconductor memory comprises a reference potential generation circuit (a reference potential setup circuit) generating a reference potential based on the information stored in the two reference memory cells (see col. 2, lines 41-57). Furthermore, Yamada et al. teach that the memory cells are fed through bit lines to an intermediate value generation (reference potential generation circuit) (see fig. 2, element 54) generates based on the information (a reference potential, i.e., an intermediate potential) received and this reference potential is fed to each of the sense amplifiers SA1-SA5 to determine whether data, stored in their corresponding memory cells, are 1 or 0 (see col. 5, lines 12-21).

As per claims **2 and 4,** Yamada et al. in figure 1(a), elements 11-15 teach that memory cells (information memory cells) storing information and the symbolic form in figure 1(a) is made up of a cell transistor and a cell capacitor as shown in detail in figure 1(b) (see col. 2, lines 23-40). Yamada et al. further, teach first/second bit lines coupled to an information memory and reference memory cells and store information and reference information in the memories (information memory and reference memory cells), first/second probe means formed of a MOS transistors detecting information on first/second bit lines and a sense amplifier having input terminals at which outputs from said first and second pre-amplification means are entered (see claims 9 and 10).

As per claim **5,** Yamada et al. teach or disclose a semiconductor memory comprising an information memory cells (see fig. 1(a) and see col. 4, lines 40-65) for storing and performing operations of reading out information, a word line for accessing the memory cell, and a reference memory cell other than the information memory cell coupled to the word line or to a

word line having the same address as the word line wherein the reference memory cell stores information for use by a sense amplifier, the information being reference information equivalent to a reference potential to the reading of information from the information memory cell (see col. 2, lines 17-40). Yamada et al. teach that a probe test carried out and a write operation of writing redundant information into a memory cell capacitor film performed when there is found a faulty redundant information memory cell (se4 col. 11, lines 20-60). Yamada et al. teach that the semiconductor memory comprises a reference potential generation circuit (a reference potential setup circuit) for generating a reference potential based on the information stored in the two reference memory cells (see col. 2, lines 41-57). Yamada et al. teach that the memory cells are fed through bit lines to an intermediate value generation (see fig. 2, element 54) and generates based on the information (a reference potential, i.e., an intermediate potential) received and the reference potential is fed to each of the sense amplifiers SA1-SA5 to determine whether data, stored in their corresponding memory cells (see col. 5, lines 12-21). Further, Yamada et al. teach that information stored in an information cell memory cell of the first memory cell group read out onto BIT LINE bit1, reference potential information stored in a reference cell 2 of the second memory cell group read out onto BIT LINE bit2 wherein the potential of BIT LINE bit1 varies (determined) depending on the stored information and further, a readout control transistor of the local probe PRBa and PRBb conduct and the potential of GLOBAL BIT LINE (Gbit1) and GLOBAL BIT LINE (Gbit2) vary depending on the potential of BIT LINE bit1 and BIT LINE bit2 and furthermore, a sense amplifier SA senses stored information and the stored and the stored information is written by a rewrite circuit into the information cell memory cell of the first memory cell group (see col. 7, lines 11-67).

As per claims **6, 7 and 9,** Yamada et al. teach or disclose a semiconductor memory comprising an information memory cells (see fig. 1(a) and see col. 4, lines 40-65) for storing and performing operations of reading out information, a word line for accessing the memory cell, and a reference memory cell other than the information memory cell coupled to the word line or to a word line having the same address as the word line wherein the reference memory cell stores information for use by a sense amplifier, the information being reference information equivalent to a reference potential to the reading of information from the information memory cell (see col. 2, lines 17-40). Yamada et al. further, teach plurality of memory cells (called information cells) arranged in a row direction coupled to a single word line WL and a plurality of information cells located in the same column coupled to a bit line wherein a local probe coupled to its corresponding bit line and acts as signal detection circuit operable to detect data on the bit line bit and furthermore, the probe coupled to one of a differential input terminal of a sense amplifiers SA of the latch type (see col. 6, lines 4-21). As for signal hold circuit is inherent to the probe means (signal detectors) because by virtue of the fact data or signals must be hold temporarily of permanently in the probe means in order to perform the process of detection and the detecting signals by the probe means or detector corresponding to the bit line bit aims to improve the quality of the transmission.

As per claim **10,** Yamada et al. teach or disclose a semiconductor memory comprising an information memory cells (see fig. 1(a) and see col. 4, lines 40-65) for storing and performing operations of reading out information, a word line for accessing the memory cell, and a reference memory cell other than the information memory cell coupled to the word line or to a word line having the same address as the word line wherein the reference memory cell stores information

for use by a sense amplifier, the information being reference information equivalent to a reference potential to the reading of information from the information memory cell (see col. 2, lines 17-40). Yamada et al. teach that a probe test carried out and a write operation of writing redundant information into a memory cell capacitor film performed when there is found a faulty redundant information memory cell (se4 col. 11, lines 20-60). Yamada et al. teach that the semiconductor memory comprises a reference a potential generation circuit (a reference potential setup circuit) generating a reference potential based on the information stored in the two reference memory cells (see col. 2, lines 41-57). Yamada et al. further, teach plurality of memory cells (called information cells) arranged in a row direction coupled to a single word line WL and a plurality of information cells located in the same column coupled to a bit line wherein a local probe coupled to its corresponding bit line and acts as signal detection circuit operable to detect data on the bit line bit and furthermore, the probe coupled to one of a differential input terminal of a sense amplifiers SA of the latch type (see col. 6, lines 4-21). As for signal hold circuit is inherent to the probe means (signal detectors) because by virtue of the fact data or signals must be hold temporarily of permanently in the probe means in order to perform the process of detection and the detecting signals by the probe means or detector corresponding to the bit line bit aims to improve the quality of the transmission.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject

matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims **3 and 8** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al. (U.S. PN: 6,091,65).

As per claim **3,** Yamada et al. teach or disclose a semiconductor memory comprising an information memory cells (see fig. 1(a) and see col. 4, lines 40-65) for storing and performing operations of reading out information, a word line for accessing the memory cell, and a reference memory cell other than the information memory cell coupled to the word line or to a word line having the same address as the word line wherein the reference memory cell stores information for use by a sense amplifier, the information being reference information equivalent to a reference potential to the reading of information from the information memory cell (see col. 2, lines 17-40). Yamada et al. teach that a probe test carried out and a write operation of writing redundant information into a memory cell capacitor film performed when there is found a faulty redundant information memory cell (se4 col. 11, lines 20-60). Yamada et al. teach that the semiconductor memory comprises a reference a potential generation circuit (a reference potential setup circuit) generating a reference potential based on the information stored in the two

reference memory cells (see col. 2, lines 41-57). Yamada et al. teach that the memory cells are fed through bit lines to an intermediate value generation (reference potential generation circuit (see fig. 2, element 54) generates based on the information (a reference potential, i.e., an intermediate potential) received and this reference potential is fed to each of the sense amplifiers SA1-SA5 to determine whether data, stored in their corresponding memory cells, are 1 or 0 (see col. 5, lines 12-21). Further, Yamada et al. teach that information, stored in an information cell memory cell of the first memory cell group read out onto BIT LINE bit1, reference potential information, stored in a reference cell 2 of the second memory cell group read out onto BIT LINE bit2 wherein the potential of BIT LINE bit1 varies (determined) depending on the stored information and further, a readout control transistor of the local probe PRBa and PRBb conduct and the potential of global bit lines vary (determined) depending on the potential of bit line bit1/bit line bit2 and furthermore, a sense amplifier SA senses stored information and the stored and information is written by a rewrite circuit into the information cell memory cell of the first memory cell group (see col. 7, lines 11-67). Yamada et al. **do not explicitly** teach a statistical process for statistically processing the value of potential. **Nevertheless,** as would have been well known to one ordinary skill in the art at the time the invention was made, such statistical process are required in order to deal with collection, analysis and interpretation masses of numerical data. **Accordingly,** it would have been obvious to one ordinary skill in the art to employ a statistical process included in the potential reference memory because such processes would have been required in order to guarantee accurate operations.

As per claim **8,** Yamada et al. teach or disclose a semiconductor memory comprising an information memory cells (see fig. 1(a) and see col. 4, lines 40-65) for storing and performing

operations of reading out information, a word line for accessing the memory cell, and a reference memory cell other than the information memory cell coupled to the word line or to a word line having the same address as the word line wherein the reference memory cell stores information for use by a sense amplifier, the information being reference information equivalent to a reference potential to the reading of information from the information memory cell (see col. 2, lines 17-40). Yamada et al. teach that a probe test carried out and a write operation of writing redundant information into a memory cell capacitor film performed when there is found a faulty redundant information memory cell (se4 col. 11, lines 20-60). Yamada et al. teach that the memory cells are fed through bit lines to an intermediate value generation (reference potential generation circuit (see fig. 2, element 54) generates based on the information received and this reference potential is fed to each of the sense amplifiers SA1-SA5 to determine the data stored in the memory cells (see col. 5, lines 12-21). Further, Yamada et al. teach a readout control transistor of the local probe PRBa and PRBb conduct and the potential of global bit lines vary (determined) depending on the potential of bit line bit1/bit line bit2 and furthermore, a sense amplifier SA senses stored information and the stored information written by a rewrite circuit into the information cell memory cell (see col. 7, lines 11-67). Yamada et al. **do not explicitly** teach a statistical process for statistically processing the value of potential. **Nevertheless,** as would have been well known to one ordinary skill in the art at the time the invention was made, such statistical process are required in order to deal with collection, analysis and interpretation masses of numerical data. **Accordingly,** it would have been obvious to one ordinary skill in the art to employ a statistical process included in the potential reference memory because such processes would have been required in order to guarantee accurate operations. Yamada et al. **do**

not explicitly teach A/D converter for converting data. **However,** the use of A/D converter in data communication is conventional and well known. **Therefore,** it would have been obvious at the time the invention was made to one of ordinary skill in the art to include an A/D converter to convert analog signal to digital signal. **One ordinary** skill in the art would have been employed A/D or D/A converters during testing of the memory device in order to ensure that all types of memories tested.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US PN: 6,597,236 Ooishi et al.

US PN: 6,009,022 Lee et al.

7. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (703) 305-7743. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for after final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Esaw Abraham

Art unit: 2133

Gregory J. Lamarre
for

Albert DeCady
Primary Examiner